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EXPRESS MAIL LABEL NO.: EL631547708US

**PATENT**

Case Docket No. 36856.336

Date: July 13, 2000

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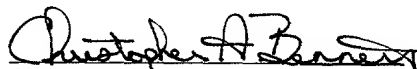
Transmitted herewith for filing is the patent application of:

**Inventor(s):** Hideaki TANAKA**For:** DELAY LINE☐ Applicant(s) claim(s) benefit under 35 U.S.C. § 119(e) of United States provisional application No. \_\_\_\_\_ filed \_\_\_\_\_**Enclosed are:**☒ 33 Pages of Specification☒ 8 Sheet(s) of drawings (☒ formal ☐ informal)☒ Declaration and Power of Attorney ☐ Will follow.☒ Form PTO-1595 and an Assignment of the invention to Murata Manufacturing Co., Ltd. of 26-10 Tenjin 2-chome, Nagaokakyo-shi, Kyoto-fu 617-8555, JAPAN ☐ Will follow☒ A certified copy of Japanese Patent Appln. No. 11-202294 filed on July 15, 1999, from which priority is claimed in the subject case pursuant to Rule 55b and 35 U.S.C. 119. ☐ Will follow.☐ A verified statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27.☐ Information Disclosure Statement, Form PTO 1449, and \_ cited reference(s).☐ Change of Correspondence Address☐ Preliminary Amendment☒ General authorization/request to Petition for Extensions of Time☒ Return Postcard

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BASIC FEE				\$345.00	OR		
TOTAL CLAIMS	22	-20=	2	\$	OR	X 18	\$690.00
INDEP CLAIMS	2	-3=	-0-	\$	OR	X 78	\$36.00
MULTIPLE				\$	OR	+ 260	\$-0-
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PRESENTED			TOTAL =			<b>TOTAL:</b>	<b>\$726.00</b>

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Respectfully submitted,

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PATENT

Docket No:36856.336

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Hideaki TANAKA

For: DELAY LINE

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CERTIFICATE OF MAILING

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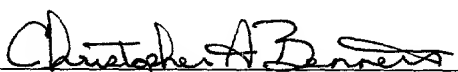
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I hereby certify that an application for patent, including:

One-page cover sheet; 33 pages of Specification (which includes 22 claims and a one-page Abstract); 8 Sheets of informal Drawings; an executed Combined Declaration and Power of Attorney; a General Authorization/Request to Petition for Extensions of Time; a Credit Card Payment Form (PTO-2038) in the amount of \$726.00 to cover the filing fee; an executed Assignment document and Form PTO 1595, along with a Credit Card Payment Form (PTO-2038) in the amount of \$40.00 to cover the assignment recordation fee; a certified Priority Document; a Transmittal Letter (Form PTO 1082); and Return Postcard are being deposited with the U.S. Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. § 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Box Patent Application, Washington, D.C. 20231.

Date of Deposit: July 13, 2000

  
Christopher A. Bennett

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## 1. Field of the Invention

## 2. Description of the Related Art

However, with the above-described conventional delay line, by merely increasing the number of windings when forming an inductor in order to increase its inductance value, or merely increasing the areas of capacitive electrodes of a capacitor in order to increase its capacitance value, there will occur a problem that the frequency characteristic (a pulse rise characteristic) of the delay line will be worsened, or a problem that the

flatness of a group delay time (waveform deflection characteristic) will be deteriorated.

#### SUMMARY OF THE INVENTION

In order to overcome the problems described above, preferred embodiments of the present invention provide a compact, very small delay line having an excellent flatness in its group delay time characteristic, and also having an excellent frequency characteristic.

According to one preferred embodiment of the present invention, a delay line includes a coil divided into at least three inductors, and at least three stages of low pass filters including the at least three inductors and a plurality of capacitors, wherein the low pass filters are contained within a laminated body defined by laminating a plurality of insulating layers.

With the above constitution, since each of the inductors and capacitors has only a small inductance value and a small capacitance value, respectively, there is little possibility that a pulse rise characteristic and a flatness of a group delay time of the delay line will be deteriorated. On the other hand, since the delay line as a whole has a large inductance value and a large capacitance value, the delay line achieves a long delay time.

Further, since coil conductor patterns constituting the

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In addition, a capacitor connected to an end of at least one of the inductors constituting the low pass filters, and another capacitor connected to another end of the at least one of the inductors, are arranged in different positions in the laminating direction of the insulating layers. In this way, the low pass filter including the inductor and the two capacitors has only a small electrostatic capacitance coupling between the two

capacitors, thereby obtaining an even flatter characteristic of a group delay time.

Further, in the delay line according to preferred embodiments of the present invention, a ratio of a vertical dimension to a lateral dimension of the coil conductor pattern is preferably approximately 1. When the coil conductor pattern has a substantially rectangular shape, the coil conductor pattern is defined as substantially a square shape, thereby making it possible to obtain a high Q.

Moreover, in the delay line according to preferred embodiments of the present invention, one end of an inductor of a k stage in the low pass filter and one end of an inductor of a k+1 stage adjacent thereto in the low pass filter are electrically connected to each other on an upper layer of the laminated body, and the other end of the inductor of the k+1 stage in the low pass filter and one end of an inductor of the k+2 stage adjacent thereto in the low pass filter are electrically connected to each other on a lower layer of the laminated body.

Adjacent inductors of adjacent low pass filters are alternately connected on the lower layer and the upper layer of the laminated body, thereby causing the magnetic fluxes of mutually adjacent inductors to be arranged in opposite directions. Due to this unique arrangement, magnetic coupling of the mutually adjacent inductors is greatly

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reduced, and cross-talk is minimized.

Other features, elements, characteristics and advantages of the present invention will become more apparent from the detailed description of preferred embodiments with reference to the attached drawings.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is an exploded perspective view schematically illustrating a first preferred embodiment of a delay line according to the present invention.

Fig. 2 is a perspective view schematically indicating an outer appearance of the delay line shown in Fig. 1.

Fig. 3 is an electric equivalent circuit diagram of the delay line shown in Fig. 2.

Fig. 4 is a graph indicating a transient response characteristic of the delay line.

Fig. 5 is a graph indicating a relationship between the group delay time and a frequency, depending on a dielectric constant of an insulating layer.

Fig. 6 is a plain view indicating the directions of magnetic fluxes passing through various inductors shown in Fig. 1.

Fig. 7 is a graph indicating a relationship between the group delay time and a frequency, depending on the directions of magnetic fluxes of the inductors.

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Fig. 8 is an exploded perspective view schematically illustrating a second preferred embodiment of a delay line according to the present invention.

Fig. 9 is a perspective view schematically indicating an outer appearance of the delay line shown in Fig. 8.

Fig. 10 is an electric equivalent circuit diagram of the delay line shown in Fig. 9.

Fig. 11 is a plain view indicating the directions of magnetic fluxes passing through various inductors shown in Fig. 8.

Fig. 12 is an exploded perspective view schematically illustrating another preferred embodiment of a delay line according to the present invention.

Fig. 13 is a perspective view schematically indicating an outer appearance of the delay line shown in Fig. 12.

#### DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Preferred embodiments of a delay line according to the present invention will be described below with reference to the accompanying drawings.

Fig. 1 is an exploded perspective view indicating a first preferred embodiment of a delay line according to the present invention. The delay line 1 is a monolithic type circuit array (as shown in Fig. 3), in which a coil has been divided preferably into four inductors L1 to L4, and four-

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Inductor L1 includes coil conductor patterns L1a to L1d provided on insulating sheets 24 to 27, and has a plurality of via holes 4 for continuously and successively connecting together the coil conductor patterns L1a to L1d. One end of the coil conductor pattern L1a corresponding to one end of the inductor L1 is connected through a via hole 4 to a connecting pattern 5 provided on an insulating sheet 23. Further, one end of the coil conductor pattern L1d corresponding to the other end of the inductor L1 is connected through a via hole 4 to a connecting pattern 8 provided on an insulating sheet 28.

Inductor L2 includes coil conductor patterns L2a, L2b, L2c and L2d provided respectively on the insulating sheets 27, 26, 25 and 24, and has a plurality of via holes 4 for continuously and successively connecting together the coil conductor patterns L2a to L2d. One end of the coil conductor pattern L2a corresponding to one end of the inductor L2 is connected through a via hole 4 to the connecting pattern 8 provided on the insulating sheet 28. Further, one end of the coil conductor pattern L2d corresponding to the other end of the inductor L2 is connected through a via hole 4 to a connecting pattern 6

Inductor L3 includes coil conductor patterns L3a to L3d provided respectively on the insulating sheets 24 to 27, and has a plurality of via holes 4 for continuously and successively connecting together the coil conductor patterns L3a to L3d. One end of the coil conductor pattern L3a corresponding to one end of the inductor L3 is connected through a via hole 4 to the connecting pattern 6 provided on the insulating sheet 23. Further, one end of the coil conductor pattern L3d corresponding to the other end of the inductor L3 is connected through a via hole 4 to a connecting pattern 9 provided on the insulating sheet 28.

Then, the coil conductor patterns L1a to L4d are all

The above described inductors L1 to L4 are arranged such that their coil conductor patterns L1a, L2d, L3a and L4d have substantially the same shapes as each other, and are arranged in a matrix array of 2 rows x 2 columns on the surface of the insulating sheet 24. Further, other coil conductor patterns preferably have substantially the same shapes and substantially the same positional relationships as those of the coil conductor patterns L1a, L2d, L3a and L4d. In this way, the coil conductor patterns L1a to L4d are efficiently arranged within the delay line 1, thereby making it possible to manufacture a delay line 1 which is very compact in size.

On the other hand, the capacitor C1 includes an insulating sheet 22, a capacitor electrode 10 disposed on the insulating sheet 22, and a capacitor electrode 12 disposed on an insulating sheet 21. The capacitor C2 includes an insulating sheet 30, a capacitor electrode 13 disposed on a sheet 29, and a capacitor electrode 16 disposed on the insulating sheet 30. The capacitor C3

Each of the insulating sheets 21 to 31, are stacked on each other, and are sintered together so as to define an integral and monolithic body, thereby providing a laminated body 35 as shown in Fig. 2. An input electrode 41, an output electrode 42 and a ground electrode 43 are respectively arranged on the left end surface, right end surface and approximate central portion of the laminated body 35. Relay electrodes 44, 45 and 46 are provided respectively on the left and right of the front surface of the laminated body 35, and on the right of the back surface of the same laminated body 35.

The input electrode 41 is connected via the connecting pattern 5 to one end (the coil conductor pattern L1a) of the inductor L1, and is also connected to the capacitor electrode 10. The output electrode 42 is connected via the connecting pattern 7 to the other end (the coil conductor pattern L4d) of the inductor L4, and is also connected to

the capacitor electrode 11. The ground electrode 43 is connected to the capacitor electrode 12 and to the capacitor electrode 16. The relay electrode 44 is connected via the connecting pattern 8 to the other end (the coil conductor pattern L1d) of the inductor L1 and to one end (the coil conductor pattern L2a) of the inductor L2, further connected to the capacitor electrode 13. The relay electrode 45 is connected via the connecting pattern 6 to the other end (the coil conductor pattern L2d) of the inductor L2 and to one end (the coil conductor pattern L3a) of the inductor L3, further connected to the capacitor electrode 14. The relay electrode 46 is connected via the connecting pattern 9 to the other end (the coil conductor pattern L3d) of the inductor L3 and to one end (the coil conductor pattern L4a) of the inductor L4, further connected to the capacitor electrode 15. Fig. 3 is an electric equivalent circuit diagram of the delay line 1 constructed in the above described manner.

Since the delay line 1 is arranged such that one coil has been divided preferably into four inductors L1 to L4, it is possible that the inductors L1 to L4 and the capacitors C1 to C5 have only small inductance values and small capacitance values, thereby making it possible to improve the pulse rise characteristic and waveform deflection characteristic of the delay line. On the other hand, since

the value of the inductance and the value of the capacitance of an entire delay line 1 are all large, it is possible to obtain a relatively long delay time. Fig. 4 is a graph (refer to a solid line 48a) indicating a transient response characteristic at a time when a trapezoidal pulse wave represented by a solid line 47 has been input into the delay line 1 (having a delay time of about 2nS) which includes four LC  $\pi$  type low pass filters F1 to F4. Here, for comparison, the graph includes both a transient response characteristic (refer to a two-dot chain line 49) of a delay line having only one stage LC  $\pi$  type low pass filter and a transient response characteristic (refer to a broken line 50) of a delay line having two-stage LC  $\pi$  type low pass filter. In fact, when using a delay line having only one stage low pass filter or two-stage low pass filter, since a pulse rise characteristic is not good and a distortion in an output waveform is large, such delay lines are difficult to be put into practical use. In contrast to this, the delay line 1 having four low pass filters and having the multiple stage arrangement in preferred embodiments of the present invention, achieves an excellent pulse rise characteristic and only a small distortion in its output waveform.

Further, a magnetic material or a non-magnetic material may be used as a material for the insulating sheets 21 to 31. When a magnetic material is used, the inductance values of

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In the first preferred embodiment, as a material for forming the insulating sheets 21 to 31, a non-magnetic material is preferably used (for example, a Ba-Al-Si ceramic dielectric material having a dielectric constant of 6 and having magnetic permeability that is almost the same as a magnetic permeability under a vacuum condition). In this manner, even if the inductors L1 to L4 are arranged very close to each other within the laminated body 35, cross-talk between the inductors L1 to L4 located adjacent to each other is prevented. As a result, the flatness of a group delay time of the delay line 1 is not deteriorated.

Here, Fig. 5 shows a simulation result of a relationship between the group delay time and the frequency characteristic of a model obtained when the dielectric constant of a non-magnetic material has been changed to various extents. In practice, the coil conductor patterns

In Fig. 5, a solid line 51 represents that a dielectric constant is 5, one-dot chain line 52 represents that a dielectric constant is 15, a broken line 53 represents that a dielectric constant is 30. As is clear from Fig. 5, if a dielectric constant is 15 or less, only a small surge or increase occurs in the relationship between the group delay time and the frequency characteristic, thereby making it possible to obtain a delay line having a more flat relationship between the group delay time and the frequency characteristic. The reason for this may be explained as follows. When a dielectric constant is low, electrostatic capacitance coupling between various layers of the coil conductor patterns L1a to L4d of the inductors L1 to L4 becomes small. Accordingly, cross-talk characteristics between the layers of coil conductor patterns L1a to L4d are minimized.

Further, in the delay line 1, as shown in Fig. 1, a second end (the coil conductor pattern L1d) of the inductor L1 in the first stage low pass filter F1, and a first end (the coil conductor pattern L2a) of the inductor L2 in the second stage low pass filter F2 are electrically connected



with each other via the connecting pattern 8 on the upper layer (the sheet 28) of the laminated body 35. A second end (the coil conductor pattern L2d) of the inductor L2, and a first end (coil conductor pattern L3a) of the inductor L3 in the third stage low pass filter F3 are connected via the connecting pattern 6 on the lower layer (the sheet 23) of the laminated body 35. Further, a second end (the coil conductor pattern 13d) of the inductor L3, and a first end (coil conductor pattern L4a) of the inductor L4 in the fourth stage low pass filter F4 are connected via the connecting pattern 9 on the upper layer (the sheet 28) of the laminated body 35.

With the above arrangement, the inductors L1 to L4 of the low pass filters F1 to F4 adjacent to each other are connected at connection positions which are alternately located on the upper layer and the lower layer within the laminated body 35. Accordingly, as shown in Fig. 6, the magnetic flux  $\phi_1$  to  $\phi_4$  of the inductors L1 to L4 adjacent to each other are arranged in mutually opposite directions. Thus, the mutually adjacent inductors L1 to L4 have only a small magnetic coupling, thus making it possible to further reduce the cross-talk. As a result, it becomes possible to obtain an even flatter relationship between the group delay time and the frequency characteristic.

In addition, as shown in Fig. 7, when the magnetic

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Further, in the delay line 1, the capacitor C1 connected on the input side of the inductor L1 of the first stage low pass filter F1, and a capacitor C2 connected on the output side of the inductor L1 are separately arranged on the lower layer and the upper layer of the laminated body 35. Similarly, the capacitor C4 connected on the input side of the inductor L4 of the fourth stage low pass filter F4, and a capacitor C5 connected on the output side of the inductor L4 are separately arranged at the upper layer and the lower layer of the laminated body 35. As a result of this unique configuration, the first stage low pass filter F1 and the fourth stage low pass filter F4 reduce an undesired electrostatic capacitance coupling between the capacitors C1, C4 on the input side and the capacitors C2, C5 on the output side. As a result, a delay line 1 having an even more excellent group delay time characteristic is

Fig. 8 is an exploded perspective view illustrating a second preferred embodiment of a delay line according to the present invention. In this delay line 61, one coil has been divided preferably into three inductors L1 to L3, defining a monolithic type circuit array (as shown in Fig. 10) that is a 3-stage circuit including three LC  $\pi$  type low pass filters F1, F2 and F3, including lumped constant inductors L1 to L3 and capacitors C1 to C4.

Inductor L1 includes coil conductor patterns L1a to L1e provided on insulating sheets 75 to 79, respectively, and a plurality of via holes 4 for continuously and successively connecting together the coil conductor patterns L1a to L1e. One end of the coil conductor pattern L1a corresponding to one end of the inductor L1 is connected through the via hole 4 to a connecting pattern 5 provided on an insulating sheet 74. Further, one end of the coil conductor pattern L1e corresponding to the other end of the inductor L1 is connected through the via hole 4 to a connecting pattern 8 provided on an insulating sheet 80.

Inductor L2 includes coil conductor patterns L2a, L2b, L2c, L2d and L2e provided respectively on the insulating sheets 79, 78, 77, 76 and 75, and a plurality of via holes 4 for continuously and successively connecting together the coil conductor patterns L2a to L2e. One end of the coil

conductor pattern L2a corresponding to one end of the inductor L2 is connected through a via hole 4 to the connecting pattern 8 provided on the insulating sheet 80. Further, one end of the coil conductor pattern L2e corresponding to the other end of the inductor L2 is connected through a via hole 4 to a connecting pattern 6 provided on the insulating sheet 74.

Inductor L3 includes coil conductor patterns L3a to L3e provided respectively on the insulating sheets 74 to 79, and a plurality of via holes 4 for continuously and successively connecting together the coil conductor patterns L3a to L3e. One end of the coil conductor pattern L3a corresponding to one end of the inductor L3 is connected through a via hole 4 to the connecting pattern 6 provided on the insulating sheet 74. Further, one end of the coil conductor pattern L3e corresponding to the other end of the inductor L3 is connected through a via hole 4 to a connecting pattern 7 provided on the insulating sheet 80.

The above described inductors L1 to L3 are arranged such that their coil conductor patterns L1a, L2e and L3a have substantially the same shapes, and are arranged in a matrix array of 1 row x 3 columns on the surface of the insulating sheet 75. Further, other coil conductor patterns preferably have substantially the same shapes and substantially the same positional relationships as those of

the coil conductor patterns L1a, L2e and L3a. In this way, the coil conductor patterns L1a to L3e are efficiently arranged within the delay line 1, thereby making it possible to manufacture a delay line 1 which is compact in size.

On the other hand, the capacitor C1 includes insulating sheets 71 and 72, and capacitor electrodes 62, 63 and 65. The capacitor C2 includes insulating sheets 81 and 82, and capacitor electrodes 66, 67 and 69. The capacitor C3 includes insulating sheets 71 and 72, and capacitor electrodes 62, 64 and 65. The capacitor C4 includes the sheets 81 and 82, and capacitor electrodes 66, 68 and 69.

The insulating sheets 70 to 83, after having been laminated one upon another, are sintered together so as to define an integral body, thus, a laminated body 35 is obtained as shown in Fig. 9. An input electrode 41, an output electrode 42 and a ground electrode 43 are respectively disposed on the left end surface, right end surface and approximate central portion of the laminated body 35. Relay electrodes 44, 46 are provided respectively on the left of the front surface of the laminated body 35, and on the right of the back surface of the same laminated body.

The input electrode 41 is connected via the connecting pattern 5 to one end (the coil conductor pattern L1a) of the inductor L1, and is also connected to the capacitor

Since the delay line 61 is arranged such that one coil has been divided preferably into three inductors L1 to L3, the inductors L1 to L3 and the capacitors C1 to C4 have only small inductance values and small capacitance values, therefore the pulse rise characteristic and waveform deflection characteristic of the delay line are greatly improved. On the other hand, since the value of the inductance and the value of the capacitance of an entire delay line 61 are all large, it is possible to obtain a

Further, in the delay line 61, as shown in Fig. 8, a second end (the coil conductor pattern L1e) of the inductor L1 in the first stage low pass filter F1, and a first end (the coil conductor pattern L2a) of the inductor L2 in the second stage low pass filter F2 are electrically connected with each other via a connecting pattern 8 on the lower layer of the laminated body 35. A second end (the coil conductor pattern L2e) of the inductor L2, and a first end (coil conductor pattern L3a) of the inductor L3 in the third stage low pass filter F3 are connected via the connecting pattern 6 on the upper layer of the laminated body 35.

In this way, the inductors L1 to L3 of the low pass filters F1 to F3 adjacent to each other are connected

Further, in the delay line 61, the capacitor C1 connected on the input side of the inductor L1 of the first stage low pass filter F1, and a capacitor C2 connected on the output side of the inductor L1 are separately arranged on the upper layer and the lower layer of the laminated body 35. Similarly, the capacitor C2 connected on the input side of the inductor L2 of the second stage low pass filter F2, and a capacitor C3 connected on the output side of the inductor L2 are separately arranged on the lower layer and the upper layer of the laminated body 35. In the same manner, the capacitor C3 connected on the input side of the inductor L3 of the third stage low pass filter F3, and a capacitor C4 connected on the output side of the inductor L3 are separately arranged on the upper layer and the lower



In the above described preferred embodiments, there have been explained three stages of low pass filters (in the second preferred embodiment) and four stages of low pass filters (in the first preferred embodiment), the present invention should not be limited to these specific preferred embodiments. It is in fact also possible to use an arrangement including more than four stages of low pass filters.

For example, as shown in Fig. 12, one coil may be divided into six inductors L1 to L6, forming a delay line 91 which includes six stages of LC  $\pi$  type low pass filters, including inductors L1 to L6 and capacitors C1 to C7. The delay line 91 includes an insulating sheet 92 in which coil conductor patterns L1a to L6d constituting inductors L1 to L6 are provided on the surface of the sheet, an insulating sheet 92 in which capacitor electrodes 102 to 110 are provided on the surface of the sheet, and an insulating sheet 92 in which connecting patterns 95 to 101 are provided

Further, in a process of manufacturing a laminated type delay line, insulating sheets are formed to have coil conductor patterns on their surfaces and are laminated one upon another, followed by a sintering treatment so that these insulating sheets are formed into an integral body.

However, a manufacturing method should not be limited by this particular method. It is in fact also possible that the insulating sheets are obtained by a sintering treatment conducted in advance. In addition, it is further possible to manufacture a laminated type delay line with the use of a method that will be explained in the following. Each insulating layer may be made of a paste-like insulating material via printing treatment. Then, the surface of each insulating layer is coated with a paste of electrically conductive material so as to form some coil conductor patterns thereon. After that, the coil conductor patterns are coated with a paste-like insulating material, so as to define an insulating layer with the coil conductor patterns

As may be understood from the above description, according to the present invention, one coil may be divided into at least three inductors, at least three stages of low pass filters includes the inductors and capacitors, thereby making it possible to greatly reduce the inductance values and the capacitance values of the inductors and the capacitors. Therefore, it is possible with preferred embodiments of the present invention to obtain a very compact, small-size delay line having an excellent flatness for a group delay time characteristic and an excellent pulse rise characteristic. Further, since the delay line as a whole has a large inductance value and a large capacitance, it is allowed to obtain a long delay time.

Further, a dielectric ceramic material having a dielectric constant of 15 or lower is used as a material for the insulating layers, so that a magnetic coupling and an electrostatic coupling between mutually adjacent inductors are reduced, thereby inhibiting an undesired surge or increase on a group delay time characteristic, thus ensuring a flat characteristic for the group delay time. The mutually adjacent inductors of mutually adjacent low pass

filters are alternately connected on the lower layer and the upper layer of the laminated body, and the magnetic fluxes of mutually adjacent inductors are directed in opposite directions. The magnetic coupling of the mutually adjacent inductors are greatly reduced, and the cross-talk is reduced. Therefore, it is possible to make even flatter the characteristic for the group delay time.

Moreover, in the delay line, a capacitor connected to an end of at least one of the inductors constituting the low pass filters, and another capacitor connected to another end of the at least one of the inductors, are arranged in different positions in the laminating direction of the insulating layers. In this way, the low pass filter including the inductor and the two capacitors has only a small electrostatic capacitance coupling between the two capacitors, thereby obtaining a further flat characteristic of a group delay time.

While preferred embodiments of the invention have been disclosed, various modes of carrying out the principles disclosed herein are contemplated as being within the scope of the following claims. Therefore, it is understood that the scope of the invention is not to be limited except as otherwise set forth in the claims.

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1. A delay line comprising:  
a coil divided into at least three inductors; and  
a laminated body including a plurality of insulating  
layers and at least three stages of low pass filters  
including said at least three inductors and a plurality of  
capacitors.

3. The delay line according to claim 1, wherein each of the at least three inductors has a coil axis that is substantially parallel with a laminating direction of the insulating layers of the laminated body, and winding directions of adjacent ones of the at least three inductors are opposite to each other.

4. The delay line according to claim 1, wherein the insulating layers are made of a dielectric ceramic material having a relative dielectric constant of about 15 or less.

5. The delay line according to claim 1, wherein one of the plurality of capacitors is connected to an end of at least one of the at least three inductors, and another of the plurality of capacitors is connected to another end of said at least one of the at least three inductors, are located at different positions in a laminating direction of the insulating layers.

6. The delay line according to claim 2, wherein a ratio of a vertical dimension to a lateral dimension of each of the coil conductor patterns is approximately 1.

7. The delay line according to claim 1, wherein one end of a first of the at least three inductors of a  $k$  stage in the low pass filter and one end of a second of the at least three inductors of a  $k+1$  stage adjacent thereto in the low pass filter are electrically connected to each other on an upper layer of the laminated body, and the second end of the another of the at least three inductors of the  $k+1$  stage in the low pass filter and one end of a third of the at least three inductors of a  $k+2$  stage adjacent thereto in the low pass filter are electrically connected to each other on a lower layer of the laminated body.

8. The delay line according to claim 1, wherein the

coil is divided into at least four inductors.

9. The delay line according to claim 1, wherein the low pass filters are LC  $\pi$  type low pass filters.

10. The delay line according to claim 2, wherein the insulating sheets have a plurality of via holes for connecting the coil conductor patterns that define the at least three inductors.

11. The delay line according to claim 2, wherein the coil conductor patterns that define the at least three inductors have the same shape.

12. The delay line according to claim 1, wherein the number of the plurality of capacitors is greater than the number of the inductors.

13. The delay line according to claim 1, wherein the insulating layers include magnetic material.

14. A monolithic circuit array including a delay line comprising:

a coil divided into at least three inductors; and

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a plurality of insulating layers stacked on each other to define a monolithic laminated body, the laminated body including at least three stages of low pass filters defined by lumped constant inductors and capacitors.

15. The monolithic circuit array according to claim 14, wherein at least three inductors and at least four capacitors are included in the at least three stages of low pass filters.

16. The monolithic circuit array according to claim 14, wherein at least four stages of low pass filters are provided in the monolithic laminated body, and at least four inductors and at least five capacitors are included in the at least four stages of low pass filters.

17. The monolithic circuit array according to claim 14, wherein the inductors are defined by a plurality of coil conductor patterns arranged on the same plane of the insulating layers of the laminated body.

18. The monolithic circuit array according to claim 14, wherein the insulating layers are made of a dielectric ceramic material having a relative dielectric constant of about 15 or less.

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20. The monolithic circuit array according to claim 17, wherein a ratio of a vertical dimension to a lateral dimension of each of the coil conductor patterns is approximately 1.

22. The monolithic circuit array according to claim 14, wherein the number of the plurality of capacitors is greater than the number of the inductors.

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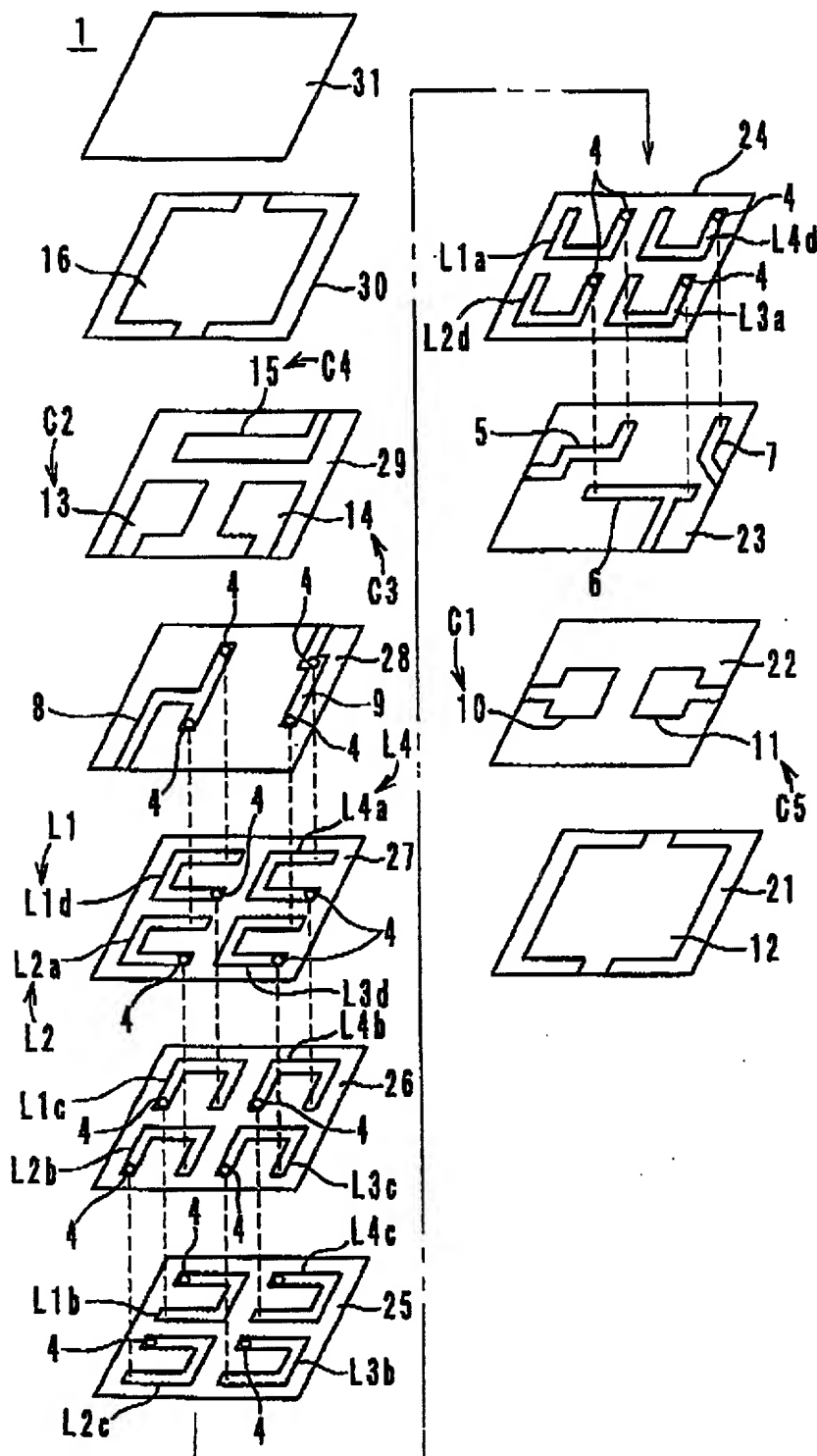
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提出日 平成11年 7月15日  
特願平11-202294

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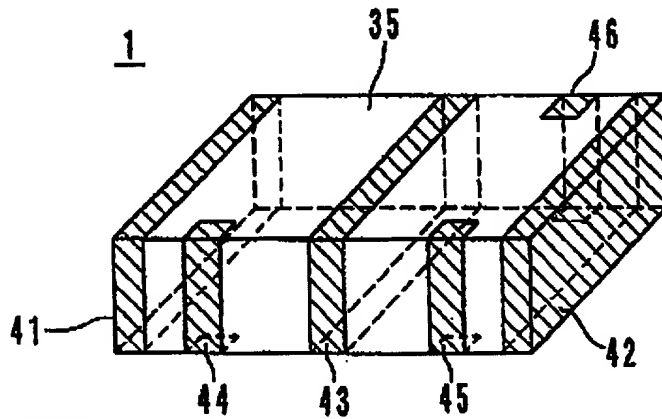
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【図1】 FIG.1

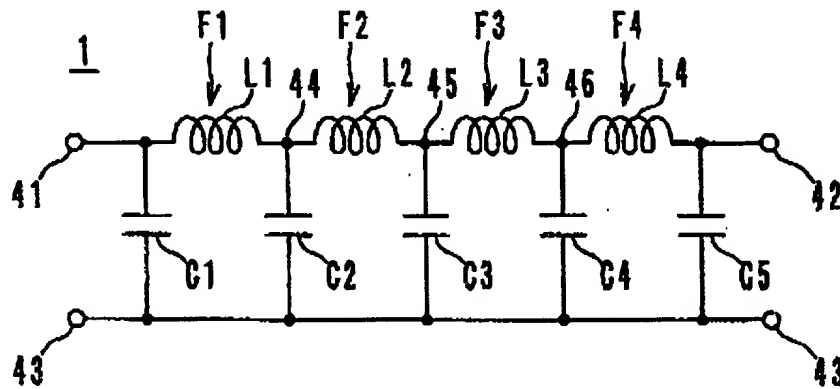


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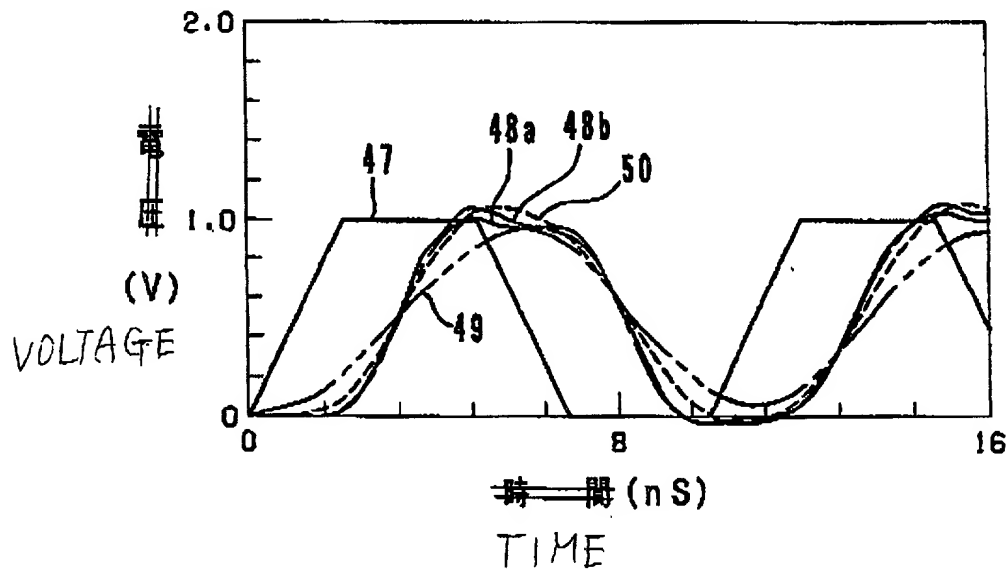
~~【図2】~~ FIG. 2



~~【図3】~~ FIG. 3



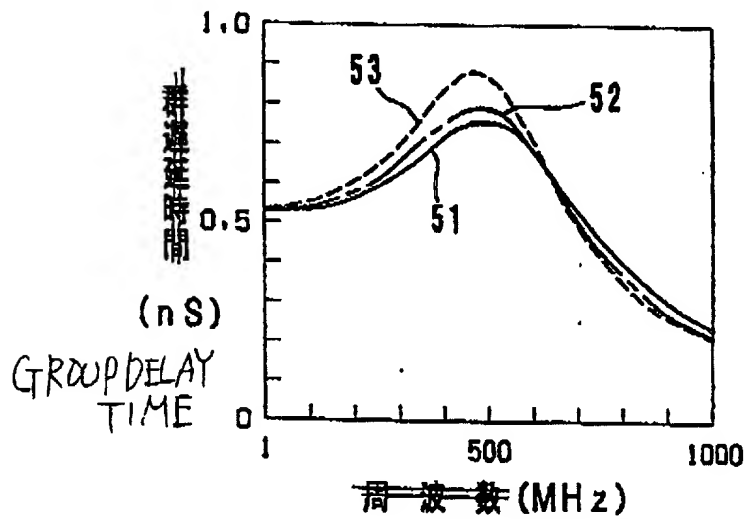
~~【図4】~~ FIG. 4



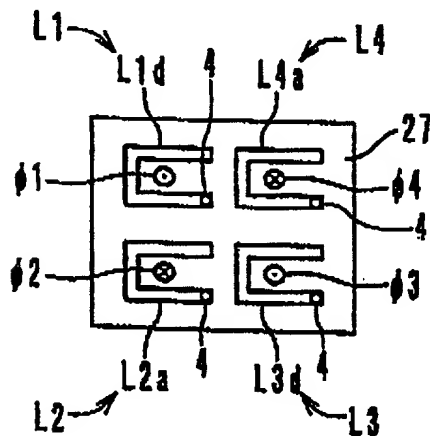
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【図5】 FIG. 5



【図6】 FIG. 6 FREQUENCY



⊗ MAGNETIC FLUX PERPENDICULAR TO THE PAPER SURFACE FROM FRONT FACE TO BACK FACE

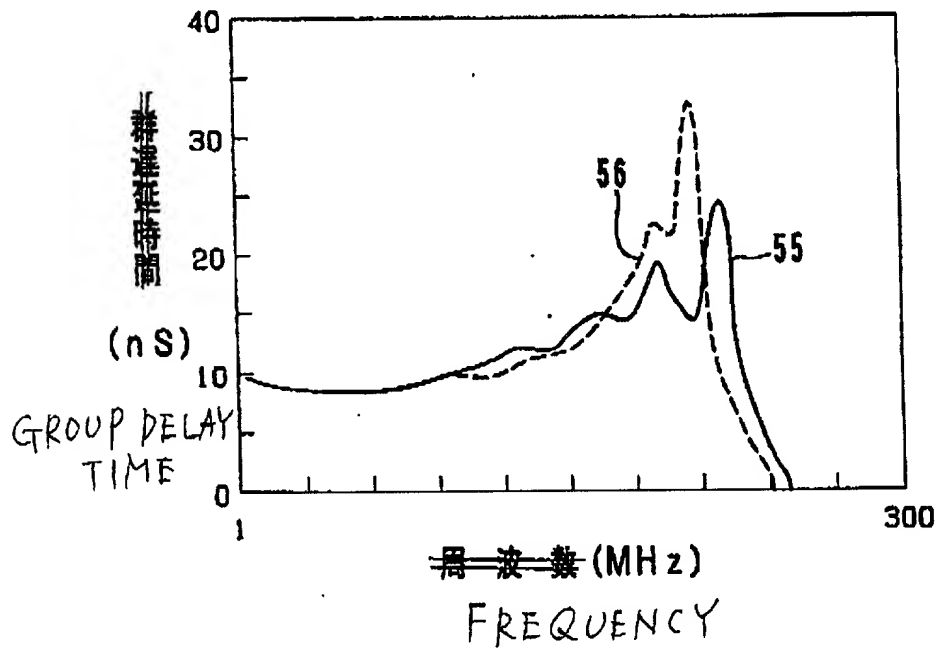
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~~図7~~ Fig. 7

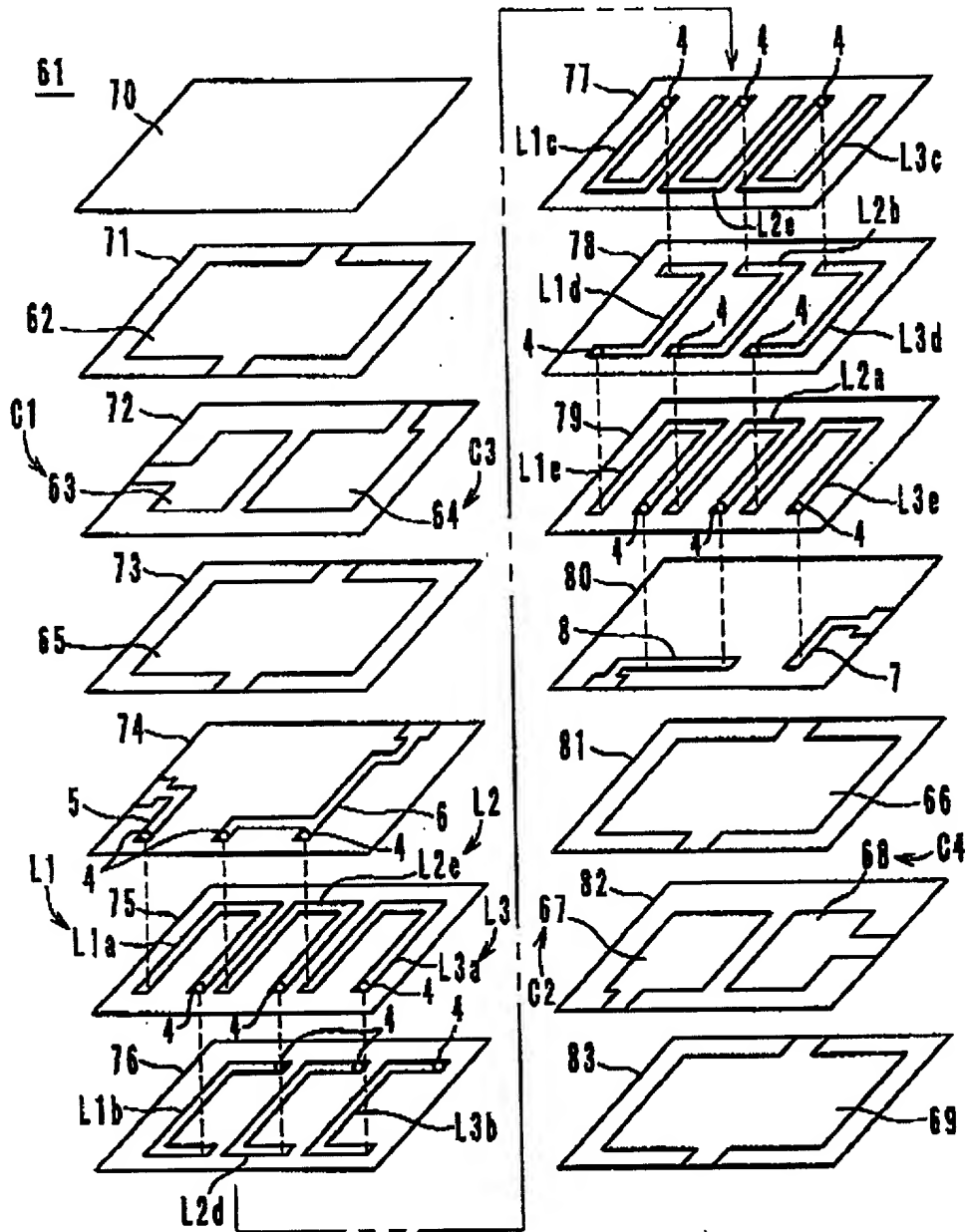
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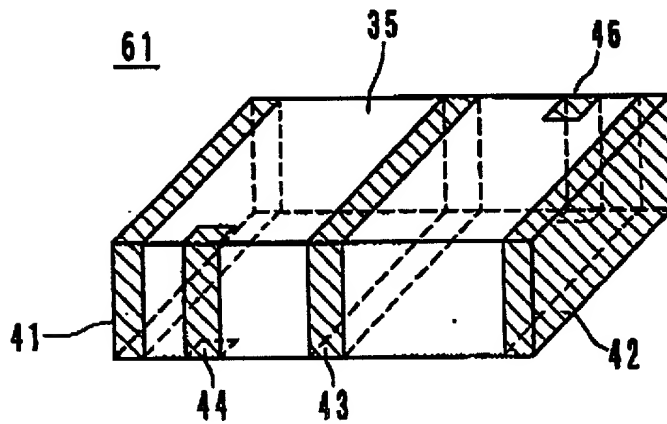
【図8】 Fig. 8



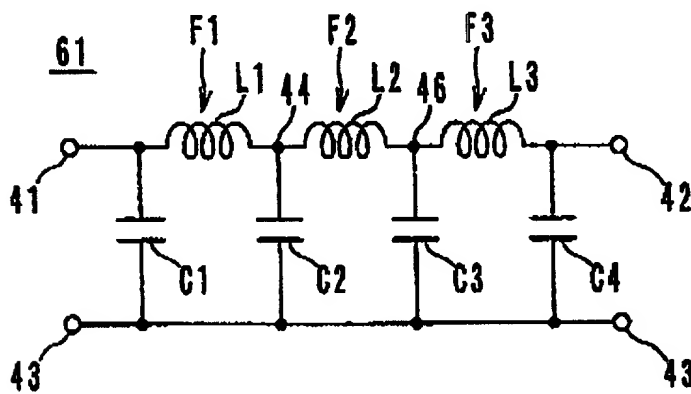


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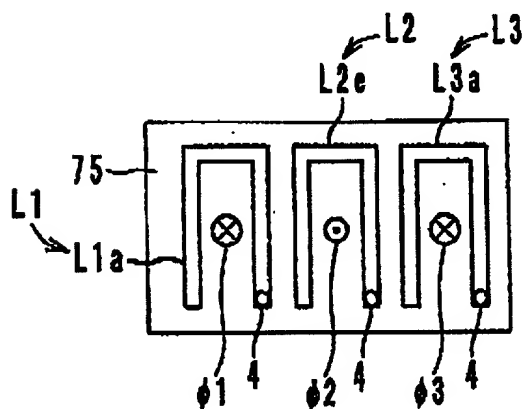
~~【図9】~~ FIG. 9



~~【図10】~~ FIG. 10



~~【図11】~~ FIG. 11

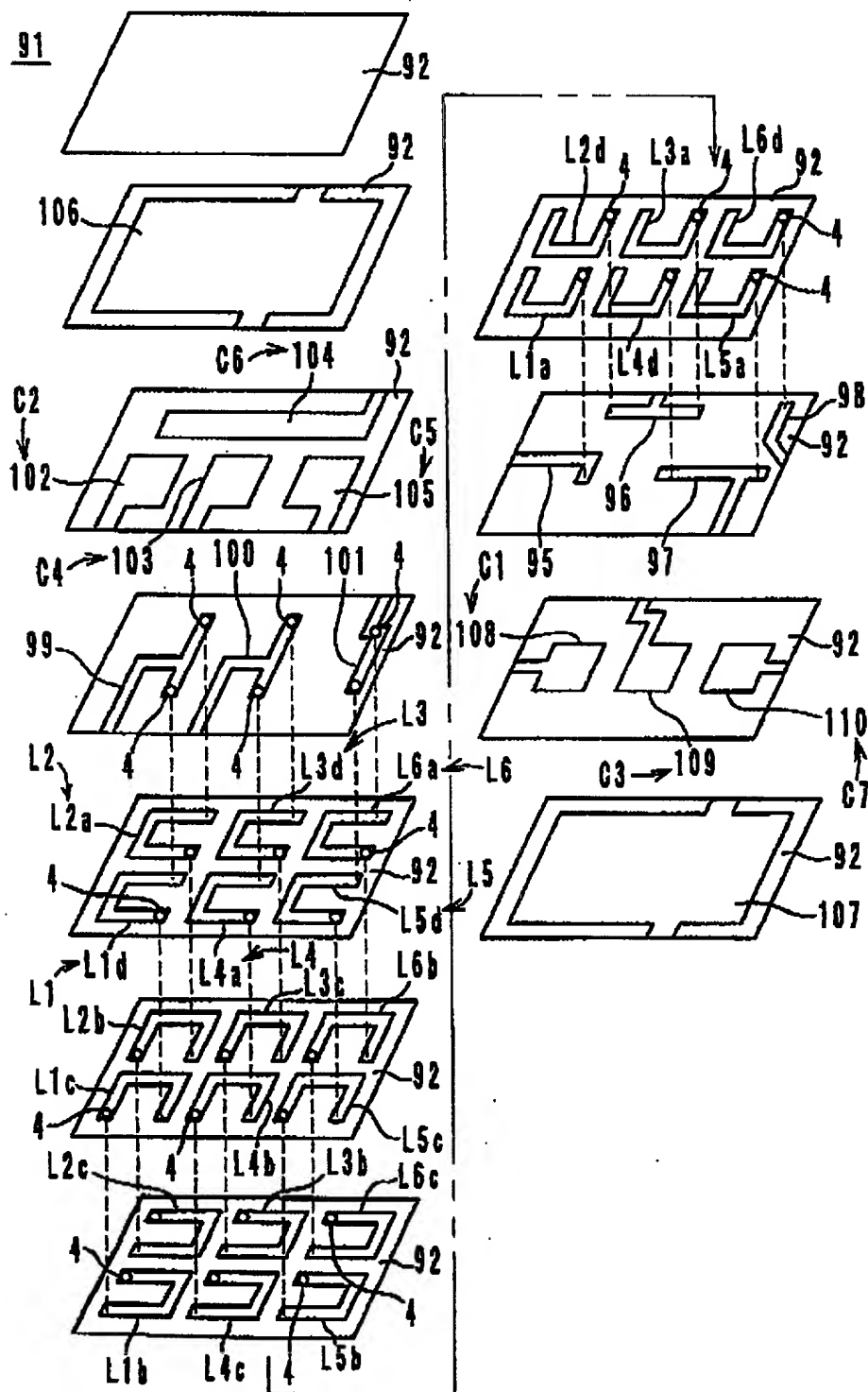


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【図12】 FIG. 12





Attorney Docket No. 36856.336

# DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **DELAY LINE** the specification of which is attached hereto unless the following box is checked:

☐ was filed on \_\_\_\_\_ as United States Application Number or PCT International Application Number \_\_\_\_\_ and was amended on \_\_\_\_\_ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)	Priority Date	Priority Claimed
11-202294 (Number)	JAPAN (Country) (PCT)	July 15, 2000 (Day/Month/Year Filed)
		Yes <input checked="" type="checkbox"/> No <input type="checkbox"/>

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

(Application Number)	(Filing Date)

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or § 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application.

(Application Number)	(Filing Date)	(Status - patented, pending, abandoned)

00615035.03100  
00615035.03100

(Application Number)

(Filing Date)

(Status - patented, pending, abandoned)

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

Joseph R. Keating, Reg. No. 37,368

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10400 Eaton Place, Suite 312  
Fairfax, VA 22030  
(703) 385-5200

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of first inventor (given name, family name) Hideaki TANAKA

Inventor's signature

Hideaki Tanaka

Date

July 11, 2000  
2000 - 7 - 11Residence Takefu-shi, Fukui-ken, JapanCitizenship JapanPost Office Address c/o Murata Manufacturing Co., Ltd., 26-10, Tenjin 2-chome, Nagaokakyo-shi, Kyoto-fu Japan

00007月13日(木) 10:06 宛先 KEATING\*BENNETT